

# designideas

READERS SOLVE DESIGN PROBLEMS

## Contact-debouncing algorithm emulates Schmitt trigger

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Among other interface problems, contact bounce complicates the connection of mechanical contacts or any noisy digital input signal to a microcontroller. Although designers have proposed a variety of hardware and software approaches that address the problems that contact bounce poses, no one has yet claimed a definitive and predictably stable approach. (For a sampling of approaches, see references 1 through 10.) The usual hardware approach to eliminating contact bounce comprises an RC filter followed by a Schmitt trigger (Figure 1). You can extend the filter's effectiveness simply by increasing the RC time constant at the expense of increased response time.

Software-debouncing methods usually include 1-bit processing, which involves twice reading the contact's input state with a fixed delay between the two readings. You can also implement a state machine or launch an input signal through a shift register and wait for three or four register-output states that haven't changed. The low efficacy of 1-bit processing approaches

stems from designers' erroneous assumptions that seemingly simple debouncing tasks can tolerate equally simple software. However, a detailed study of many types of contacts reveals a range of complex and sometimes unexpected behaviors. This Design Idea documents a more comprehensive method that can easily handle all mechanical contact interfacing to microcomputers.

The debouncing method applies full 8-bit-processing and digital-filtering techniques to digital inputs. Using as few as 20 assembly-language instructions that execute in 19 machine cycles on an ATmega8 microcontroller, the method produces a robust debouncing action (see Listing 1 at the Web version of this Design Idea at [www.edn.com/edn050707di1](http://www.edn.com/edn050707di1)).

The software closely simulates the hardware circuit in Figure 1 by using a first-order, recursive, digital lowpass filter followed by a software Schmitt trigger. In contrast to 1-bit software debouncers that generally do not apply processing to inputs, this debouncing algorithm is effective because it

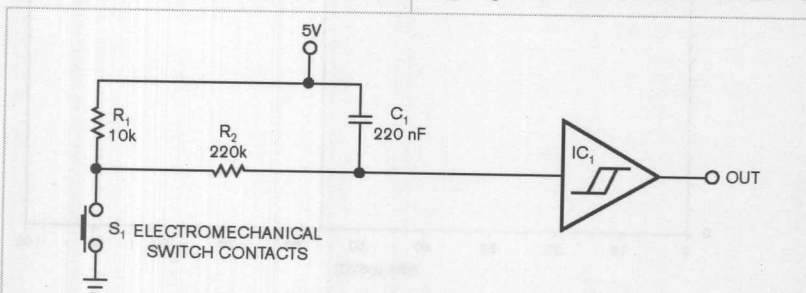


Figure 1 A basic switch-contact debouncer consists of an RC network followed by a Schmitt-trigger circuit.

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“remembers” past input transitions and assigns a “weight” to each transition depending on how long ago it occurred. Furthermore, you can alter the filter’s settings on the fly to meet changing conditions by modifying its thresholds and hence its execution time, or time constant, from the main program. The basic recursion algorithm comprises present output value =  $(1/4) \times \text{input value} + (3/4) \times \text{previous output value}$ , or,  $Y_{\text{NEW}} = (1/4) \times X_{\text{NEW}} + (3/4) \times Y_{\text{OLD}}$ .

To avoid register overflow and instability, the value of  $Y_{\text{OLD}}$  and  $X_{\text{NEW}}$  must be less than 1, which for an 8-bit microprocessor translates to values of less than 256 for  $X_{\text{NEW}}$  and  $Y_{\text{OLD}}$ . Consequently, the input  $(1/4 \times X_{\text{NEW}})$  to the filter is either 0 or 63. You then apply the output value,  $Y_{\text{NEW}}$ , to the software Schmitt trigger. The trigger uses the following algorithm: If  $Y_{\text{NEW}} > \text{hi}$ , and  $\text{flag} = 0$ , then  $\text{flag} = 1$ , and  $\text{out} = 1$ . If  $(Y_{\text{NEW}} < \text{lo})$ , and  $\text{flag} = 1$ , then  $\text{flag} = 0$ , and  $\text{out} = 0$ .

Hardware Schmitt triggers typically have fixed thresholds of one-third and two-thirds of the power-supply voltage. However, the software allows widening these thresholds and thus increasing the filter’s time constant. In operation, a timer-interrupt routine should execute the debouncing program every 4 to 5 msec. Because one time constant equals the period of one interrupt, using thresholds of 15 and 240 causes the routine’s output to “trigger” after 11 interrupts, or 44 to 55 msec, which ade-

quately processes most switches' contact bounce.

You can easily modify the main filter coefficient to provide different filtering-time constants. For particularly troublesome contact bounce, you can use the following recursion formula, which requires 16 time constants to trigger the software Schmitt routine.  $Y_{NEW} = (1/16) \times X_{NEW} + (15/16) \times Y_{OLD}$ . You can implement this algorithm with only eight assembly-language instructions, whereas the Schmitt-trigger routine requires 12 instructions. When you combine both of these routines, the software Schmitt trigger updates bit 0 of a register, which the main program loop should continuously check to ascertain the contact's status. As an alternative, you can activate a software interrupt to signal a contact's status change. To do so in the AVR architecture, you write to that port bit that functions as an external interrupt input.

Always avoid connection of mechanical contacts to interrupt inputs unless the contacts undergo hardware debouncing. Otherwise, the contacts may bounce dozens of times, unnecessarily consuming processor-machine cycles. The software routine reads the inputs only every 4 msec and thus imposes additional filtering on the inputs. Simulation and practical testing have confirmed that the debouncing algorithm behaves as expected, producing clean output transitions when enduring noisy contacts. When you program the assembly-language source code accompanying this Design Idea into an Atmel Atmega8, the code turns on an output LED connected to Port\_B bit 0 when Port\_D bit 0 of the microcontroller goes to ground.

A simulated input waveform (pind0) and its corresponding output log file (portb0.log, both available at the Web version of this Design Idea at [www.edn.com/050707di1](http://www.edn.com/050707di1)), illustrate the filter's excellent debouncing capabilities. Beginning with a key closure at 10 msec, the stimulus loads into the AVR Studio integrated development environment. After multiple input transitions, the output-log file shows a single output transition occurring at

55.333 msec. The software effectively filters out the three input pulses starting at 56.1 msec (figures 2 and 3). **EDN**

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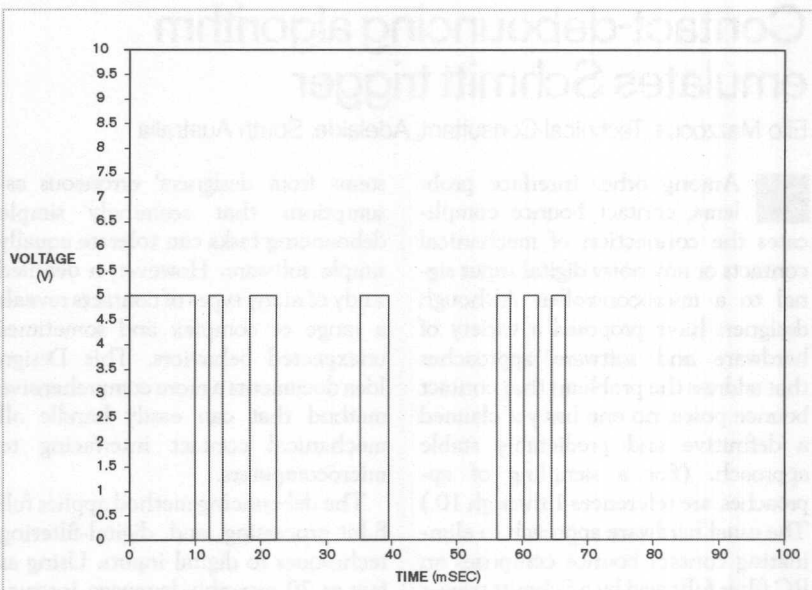


Figure 2 Switch contacts first close at 10 msec and then bounce erratically for more than 50 msec before reaching a stable closed condition.

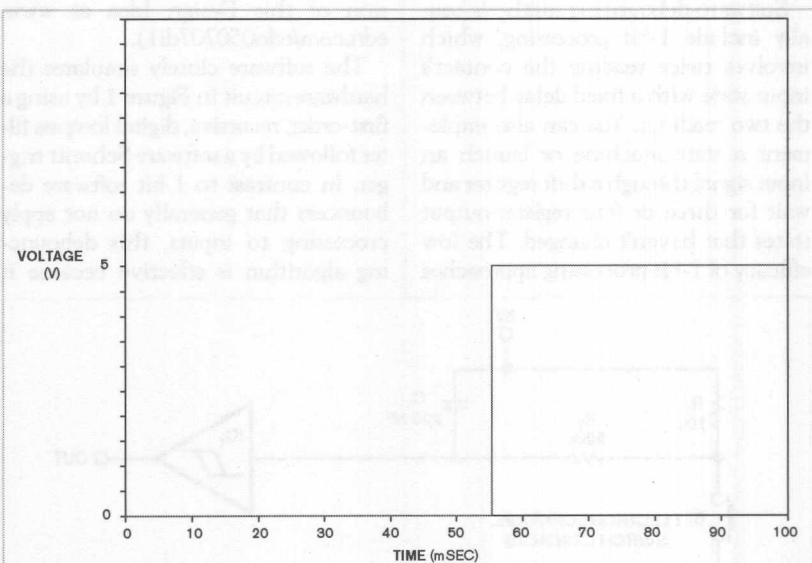


Figure 3 The debouncing-software routine signals that the contacts have closed only after bouncing ceases.

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## Inexpensive peak detector requires few components

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Requiring no rectifier diodes, the positive peak-detector circuits in figures 1 and 2 exploit the open-drain output of a Texas Instruments TLC372 fast comparator, IC<sub>1</sub>. Both versions of the detector are simple and inexpensive and provide a buffered, low-impedance output at V<sub>OUT</sub>. In addition, the TLC372's high typical input impedance of 10<sup>12</sup>Ω eliminates any need for an input buffer stage. As Figure 1 shows, the detector's output voltage at the output of op amp IC<sub>2A</sub> applies a feedback signal for the comparator and acts as a reference level for comparison with the input signal's amplitude. Upon first application of input signal V<sub>IN</sub>, the voltage on the hold capacitor, C<sub>1</sub>, is 0V, and V<sub>OUT</sub> is also 0V.

When the input signal goes more positive than the output voltage, the comparator's internal output MOSFET turns on and sinks current through R<sub>1</sub>. Provided that R<sub>2</sub> is relatively large, charging current flows into C<sub>1</sub> from IC<sub>2A</sub>'s output. Over several cycles of the input signal, the charge on C<sub>1</sub> builds up, and V<sub>OUT</sub> rises to the point at which it slightly exceeds the peak level of V<sub>IN</sub>. For as long as V<sub>OUT</sub> is slightly greater than V<sub>IN</sub>, IC<sub>1</sub>'s output MOSFET remains off, and C<sub>1</sub> receives no additional packets of charge.

As a consequence, the charge stored on C<sub>1</sub> starts to dissipate as the capacitor discharges through R<sub>2</sub> and through the bias-current path into IC<sub>2A</sub>'s inverting input. V<sub>OUT</sub> gradually falls until it is just below the peak level of V<sub>IN</sub>. The next positive peak of V<sub>IN</sub> trips comparator IC<sub>1</sub>, which pulls current through R<sub>1</sub>, "topping up" the charge on C<sub>1</sub>. This process produces a dc level at V<sub>OUT</sub> that closely approximates the positive peak level of the input waveform. The values of R<sub>1</sub>, R<sub>2</sub>, and C<sub>1</sub> determine

the ripple voltage present on V<sub>OUT</sub>.

IC<sub>2A</sub>'s inverting input is held at virtual ground potential, so whenever IC<sub>1</sub>'s output MOSFET turns on, the voltage across R<sub>1</sub> approximately equals the negative-supply-rail voltage, -V<sub>S</sub>. Therefore, using a small value of R<sub>1</sub> injects a relatively large pulse of current into C<sub>1</sub>, thus allowing the circuit to respond quickly to a sudden increase in input-signal amplitude—that is, a "fast-attack" response. However, if the value of R<sub>1</sub> is too small, the positive-going ripple on V<sub>OUT</sub> becomes excessive and can lead to bursts of oscillation around peak values of V<sub>IN</sub>.

For a given value of R<sub>2</sub>, the value of C<sub>1</sub> determines the circuit's "delay time."

(continued on pg 92)

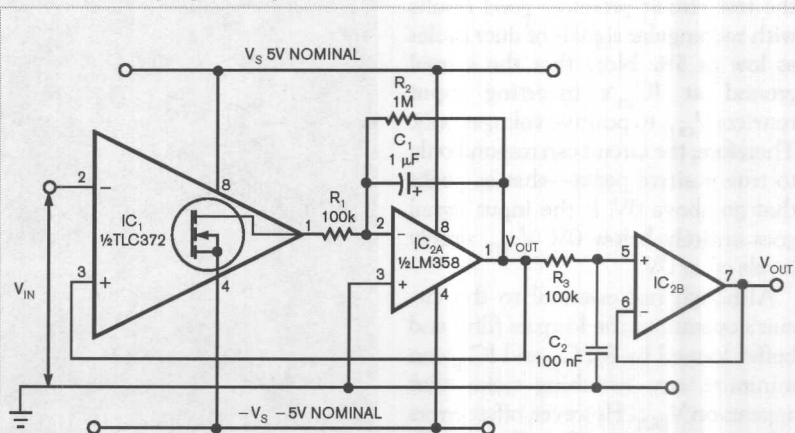


Figure 1 The dual-power-supply-voltage version of this positive peak detector requires only two active devices: a comparator and a dual operational amplifier.



A relatively large value of capacitance minimizes the negative-going ripple on  $V_{OUT}$ , which can be useful when dealing with low frequencies, low-duty-cycle pulse trains, or both. However, making  $C_1$  too large renders the detector sluggish when responding to a sudden decrease in input-signal amplitude. Note that  $C_1$  also affects the attack time; for example, doubling the capacitance doubles the time the circuit takes to acquire the peak level of  $V_{IN}$ .

Because the comparator's feedback path includes op amp  $IC_{2A}$ , offsets and errors that  $IC_{2A}$  presents have no effect on the circuit's accuracy. At low to moderate frequencies, only the comparator's input offset errors contribute to the detector's overall accuracy. At high frequencies, the comparator's response time becomes a significant factor, leading to a reduction in  $V_{OUT}$  that worsens as the frequency increases. Despite these limitations, the circuit performs well over several decades of frequency from approximately 50 Hz to 500 kHz. Figure 2 and Table 1 show the test circuit's sine-wave-frequency response by plotting the error in  $V_{OUT}$  for three peak levels of  $V_{IN}$ .

The oscilloscope photo shows the circuit's response to a 500-mV peak sine wave at 400 kHz, in which the output voltage, at 488 mV, lies just below the positive peaks (Figure 3). In addition to exhibiting good sine-wave response, the test circuit produces good results with rectangular signals of duty cycles as low as 5%. Note that the virtual ground at  $IC_{2A}$ 's inverting input restricts  $V_{OUT}$  to positive voltages only. Therefore, the circuit can respond only to true positive peaks—that is, peaks that go above 0V. If the input signal goes entirely below 0V,  $V_{OUT}$  simply levels off at 0V.

Although not essential to the circuit's operation, the lowpass filter and buffer formed by  $R_3$ ,  $C_2$ , and  $IC_{2B}$  can minimize any switching noise that appears on  $V_{OUT}$ . However, offset errors inherent to op amp  $IC_{2B}$  affect the filter's output voltage.

Figure 4 shows a single-supply version of the circuit, in which  $R_A$  and  $R_B$  set a reference voltage,  $V_{REF}$ , at  $IC_{2A}$ 's

**TABLE 1 SINE-WAVE-FREQUENCY RESPONSE**

| Frequency (Hz) | Error $V_{IN}=2.5V$ peak (%) | Error $V_{IN}=250$ mV peak (%) | Error $V_{IN}=25$ mV peak (%) |
|----------------|------------------------------|--------------------------------|-------------------------------|
| 200            | -0.4                         | 0.8                            | 10                            |
| 2000           | -0.4                         | 1.2                            | 10                            |
| 20,000         | 0                            | 0.4                            | 6.4                           |
| 200,000        | 0                            | -2.4                           | -7.6                          |
| 400,000        | 0                            | -4                             | -22                           |
| 500,000        | -2.4                         | -4.8                           | -28.4                         |
| 600,000        | -12                          | -6                             | -34                           |

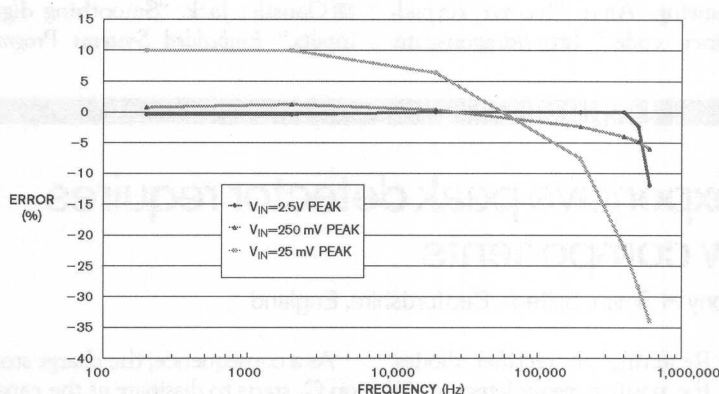


Figure 2 Plotting the difference between peak signal levels and output voltage for three peak levels illustrates the detector's frequency response.

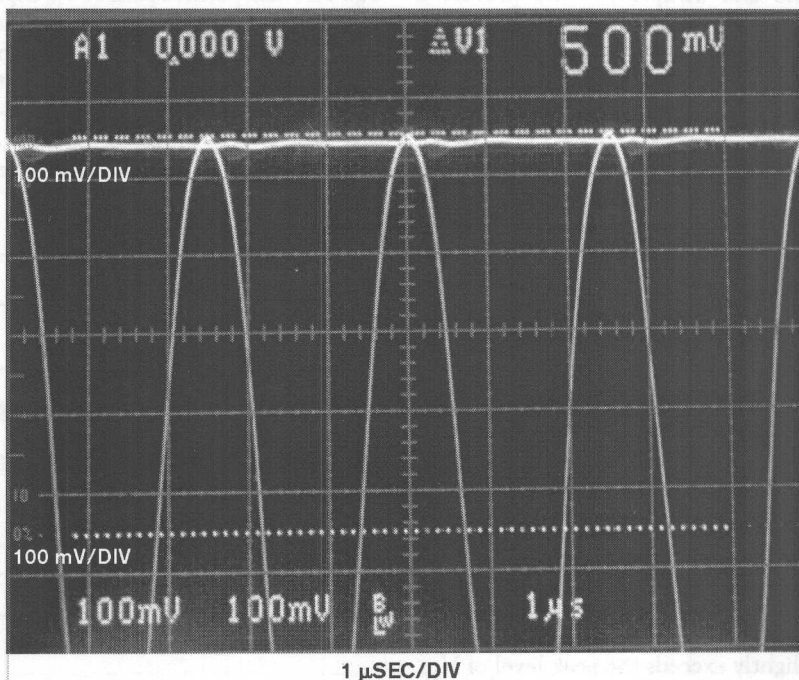


Figure 3 An oscilloscope photo displays input versus output voltages for a 400-kHz, 500-mV sine wave.